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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHU, GABRIEL L	
ART UNIT	PAPER NUMBER
2114	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/628,769	MARISETTY ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *89-109* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *89,90,92 and 101-109* is/are allowed.

6)☒ Claim(s) *91,93,94,96 and 98-100* is/are rejected.

7)☒ Claim(s) *95 and 97* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 91, 96, 98-100 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Referring to claim 91, "the CPU" has no antecedent basis.

4. Referring to claim 96, "the second firmware error handling routine has no antecedent basis.

5. Referring to claim 98, and consequently claims 99 and 100, "the... second firmware error handling..." does not have antecedent basis.

Claim Objections

6. Claim 109 objected to because of the following informalities: Referring to claim 109, "handling routine is to..." Applicant may refer to previous actions concerning this particular type of grammatical error. Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 93, 94 rejected under 35 U.S.C. 103(a) as being unpatentable over US 5862308 to Andress et al. and Official notice.

9. Referring to claim 93, Andress discloses a processor (Figure 1, elements 2, 22.); a first memory coupled to the processor (A processor comprising firmware, from line 59 of column 1, "The logical design of modern CPUs, particularly mainframes, is enormously complex. Inevitably, logic design errors are present as the design process proceeds. If the specific hardware in which a design error is discovered is still in development, it can simply be corrected, sometimes with appropriate changes in firmware. However, if the faulting condition occurs so rarely and is so elusive that it is only discovered after systems have been installed for commercial and/or other field operation, the correction of the hardware /firmware (for example, by replacing an integrated circuit having the design error with one in which the error has been corrected) can be time consuming."), the first memory to store at least a first firmware error handling routine to be invoked by the processor to attempt to correct a detected error (Figure 6, a fault identified in CPU hardware is passed to CPU firmware for correction.) when the processor cannot correct the detected error (From line 1 of column 7, "Specific faults to be intercepted are established during the initialization of the CPU 68 within its firmware 69. Thus, the Intercept flag can be set on any fault as determined to be necessary by the current processor firmware 69.").

Although Andress does not specifically disclose a display coupled to the processor, this is very well known in the art. Examiner takes official notice for a computing system comprising a monitor. A person having ordinary skill in the art at the

time of the invention could have been motivated to include a monitor because it displays things so that a user may see them.

10. Referring to claim 94, Andress discloses the first firmware error handling routine is to save a status of the detected error and at least a portion of the processor's state information (From claim 1, "A) employing, when a central processor fault occurs during an operation, a modifiable central processor firmware, which firmware is configured to recognize a central processor fault which is due to a known hardware design error and which firmware is reconfigured after the known hardware design error has been corrected to eliminate monitoring for faults due to the known hardware design error, for: i. sensing said central processor fault; ii. selectively setting, while establishing a safestore frame, an intercept flag if the fault is to be directed to a preprocessor; iii. establishing said safestore frame which includes information identifying the type of fault and whether the intercept flag is set; and iv. transferring control to the operating system fault handling module;". Abstract, "a safestore frame which includes information identifying the type of fault and whether the intercept flag is set". Line 50 of column 2, " a safestore memory for storing the contents of the plurality of software visible registers, after a data manipulation operation, in order to facilitate restart after a detected fault by transferring the corresponding contents of the safestore memory back to the software visible registers during recovery from the detected fault." Further, lines 30-35 of column 8 describing data of a safestore frame.).

Allowable Subject Matter

11. Claims 89, 90, 92, 106-109, 101-105 allowed.

12. The following is an examiner's statement of reasons for allowance: Referring to claim 89, 90, 92, 106-109, 101-105, the prior art does not teach or fairly suggest a first interface to a first memory external to the processor that stores a set of procedures to access the processor across different processor implementations and at least a first software error handling routine to be invoked by the processor via the first interface when the second logic cannot correct the detected error, in the scope and context of claim 89.

13. Referring to claims 101-104, see previous action.

14. Referring to claim 105, the prior art does not teach or fairly suggest a first external interface to a first memory that stores at least a first software error handling routine to be invoked by the processor via the first interface when the second logic cannot correct the detected error and a second software error handling routine to be invoked by the processor when the first software error handling routine cannot correct the detected error, in the scope and context of claim 105.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

15. Claims 95, 97 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. Referring to claim 95, the prior art does not teach or fairly suggest, the first memory further to store a second firmware error handling routine to be invoked by the processor to attempt to correct the detected error when the first firmware error handling routine cannot correct the detected error, in light of the parent claims.

17. Referring to claim 97, the prior art does not teach or fairly suggest, the first memory further to store a second firmware error handling routine to be invoked by the processor after the first firmware error handling routine has been invoked, in light of the parent claim.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See notice of references cited.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Gabriel L. Chu/
Primary Examiner
Art Unit 2114

gc